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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/910,684	07/20/2001	Michael Y.T. Hwang	018170002600	2529

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EXAMINER	
VO, TUNG T	

ART UNIT	PAPER NUMBER
2613	

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/910,684	HWANG ET AL.	
	Examiner	Art Unit	
	Tung T. Vo	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-9,12,14-18 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9,12,14-18 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 12, lines 3-4, "a reference frame memory for storing and supplying a block of pixels associated with a reference block from a reference frame memory" is indefinite. Does a reference frame memory store and supply a block of pixels from a reference frame memory? Appropriation correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 4-9, 12, 14-18, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Anesko et al. (US 5,987,178) as set forth in the previous Office Action dated 06/04/2004, and the discussion follows.

Re claims 1 and 12 (amended claims 1 and 12), Anesko discloses an apparatus for carrying out the method comprises:

a reference frame memory (32 of fig. 7, e.g. the memory I/O is connected to the random access memory (RAM) that is considered as a reference memory, see also col. 6, lines 20-22) for storing and supplying a block of pixels (fig. 9, 8x8 block of pixels) associated with a reference block blocks (cols. 7 and 8, e.g. pixels represent reference block data, see fig. 9); wherein said block of pixels includes NxM pixels wherein N represents the number of pixels in each row of the reference block (fig. 9, 8x8 pixels, block of pixels) and wherein M represents the number of pixels in each column of the reference block (fig. 9, 8x8 pixels).

a stage memory (51 of fig. 8) for storing said NxM pixels (55 of fig. 8);

an address translator (64 of fig. 8) for rearranging (rotating) NxM pixels so as to form P groups each having L pixels (fig. 13) such that during each read access cycle all L pixels of different one of the P groups is read from the staging memory (55 of fig. 8) to a temporary memory (PE array has memory it self called a temporary memory, see col. 7, lines10-20; e.g. the pixels represent reference block data are stored in the array itself); wherein each group of L pixels (fig. 13, e.g. s(0,i)...s(15,i) is rotated to form a rotated reference pixels (pels) r(0,1), r(0,7)) having a new row or new column of said block of pixels (fig. 13, e.g. 1st stripe, s(0,i)...s(7,i) is rearranged to r(00)...r(07), the rearranging process is performed by the array control (64 of fig. 8));

an addressing unit for providing a block of pixels in parallel from said staging memory to said temporary memory (53, 61, 66, 67 of fig. 8; see also 55, 52 of fig. 10, e.g. the block of pixels are in parallel).

Re claims 2 and 17, Anesko further discloses wherein said temporary memory (52 of fig. 8, e.g. the array is storing the block of pixels itself) is coupled to a processing unit (PE array, 52 of fig. 8) for comparing said block of pixels to a second block of pixels (col. 7, lines 11-40; see also 70 of fig. 10, e.g. ADS PE for comparing the block of pixels to a second bock of pixels).

Re claim 16, Anesko further discloses wherein said temporary memory is a two-dimensional shift register, and wherein the L pixels in each of the P groups corresponds to a new row or column of said block of pixel (fig. 13).

Re claims 4 and 18, Anesko further discloses wherein said processing unit performs a comparison for a motion estimation algorithm (col. 7, lines 20-32).

Re claims 5 and 14, Anesko further disclose wherein said staging memory (55 of fig. 8) comprises banks of memories (8 banks of staging memory 55 as shown in fig. 8), each bank providing a different one P group of pixels (col. 7, lines 50-57, e.g. 10, 8 bits, pixels array).

Re claim 6, Anesko further discloses wherein the L pixels of each group is one of a row or column rearranged pixels (fig. 13, e.g. row stripes).

Re claim 7, Anesko further discloses a search pattern that can be executed by loading said temporary memory, in a single cycle, with pixels to provide a next block to be searched (col. 7, lines 11-20; and col. 9, lines 7-26).

Re claim 8, Anesko further discloses wherein said search pattern is one of a spiral, horizontal and vertical search pattern (figs. 11 and 13, e.g. horizontal search)

Re claims 9 and 13, Anesko further discloses wherein said rearranging of said pixels comprises reordering said pixels in each row so that each pixels from a single column are spread across a plurality of columns so that they can be accessed in parallel (col. 4, lines 42-48, e.g. the memory and PE array provide a pipelining mechanism that provides the ability to rotate the reference block within the array while it is running, and simultaneously read the memory contents into the array using a dual addressing mechanism; see also col. 7, lines 21-32).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Anesko et al. (US 5,987,178) as applied to claim 12, and further in view of Kalapathy (US 5,799,169).

Re claim 15, Anesko teaches the staging memory (55 of fig. 8) but Anesko does not particularly disclose the staging memory comprises SRAM memory as claimed.

However, Kalapathy teaches a SRAM memory is used in the motion estimation (111 of fig. 1). Therefore, taking the teachings of Anesko and Kalapathy as a whole, it would have

been obvious to one of ordinary skill in the art to incorporate the SRAM (111 of fig. 1) of Kalapathy into the motion estimator of Anesko for the same purpose to storing the new pixels to be updated. Doing so would allow the CPU to indicate that immediate processing of the queued instructions is advantageous in order to avoid unnecessary stalls.

1. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Anesko et al. (US 5,987,178) as applied to claim 19, and further in view of Maturi et al (US 5,731,850).

Re claim 20, Anesko teaches the search left to right and top to bottom as shown in column 9, +/-1 search pattern but Anesko does not particularly four buffers coupled to said two dimensional shift register for buffering new rows and columns of pixels to be shifted in from the left, right, top and bottom as claimed.

However, Maturi teaches four buffers coupled to said two dimensional shift register for buffering new rows and columns of pixels to be shifted in from the left, right, top and bottom (col. 9, lines 30-67, e.g. 4 registers store the f.sub.-- codes used to determine the motion estimation search ranges for B-frames which are located 2, 3 or 4 frames). Therefore, taking the combined teachings of Anesko and Maturi as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the teachings of Maturi into the motion estimator of Anesko for the same purpose of performing the left, right, top, and bottom search. Doing would take advantage of the high-resolution capability of a hierarchical block matching motion estimation.

Response to Arguments

2. Applicant's arguments filed 10/07/04 have been fully considered but they are not persuasive.

The applicant argued that there is not disclosure of Anesko of " retrieving block of pixel...corresponds to a new row or column of said block of pixels" specified in claims 1 and 12, page 6 of the remarks.

The examiner respectfully disagrees with the applicant. It is submitted that Anesko clearly discloses an apparatus for carrying out the method comprises a reference frame memory (32 of fig. 7, e.g. the memory I/O is connected to the random access memory (RAM) that is considered as a reference memory, see also col. 6, lines 20-22) for storing and supplying a block of pixels (fig. 9, 8x8 block of pixels) associated with a reference block blocks (cols. 7 and 8, e.g. pixels represent reference block data, see fig. 9); wherein said block of pixels includes NxM pixels wherein N represents the number of pixels in each row of the reference block (fig. 9, 8x8 pixels, block of pixels) and wherein M represents the number of pixels in each column of the reference block (fig. 9, 8x8 pixels); a stage memory (51 of fig. 8) for storing said NxM pixels (55 of fig. 8); an address translator (64 of fig. 8) for rearranging (rotating) NxM pixels so as to form P groups each having L pixels (fig. 13) such that during each read access cycle all L pixels of different one of the P groups is read from the staging memory (55 of fig. 8) to a temporary memory (PE array has memory it self called a temporary memory, see col. 7, lines10-20; e.g. the pixels represent reference block data are stored in the array itself); wherein each group of L pixels (fig. 13, e.g. s(0,i)...s(15,i) is rotated to form a rotated reference pixels (pels) r(0,1), r(0,7)) having a new row or new column of said block of pixels (fig. 13, e.g. 1st stripe,

s(0,i)...s(7,i) is rearranged to r(00)...r(07), the rearranging process is performed by the array control (64 of fig. 8)); an addressing unit for providing a block of pixels in parallel from said staging memory to said temporary memory (53, 61, 66, 67 of fig. 8; see also 55, 52 of fig. 10, e.g. the block of pixels are in parallel). Therefore, Anesko anticipates the claimed features.

The applicant further argued that Anesko fails to disclose reading the columns of pixels, pages 6-7 of the remarks.

The examiner respectfully disagrees with the applicant. It is submitted that Anesko clearly discloses reading (loading) the columns of pixels (COL LOAD, COL CHANGE of fig. 10, see also col. 7, lines 62-col.8, line 30, wherein the PE array performs the metrics over the block, which means 8x8 reference blocks is read out for the PE array, 8x8 reference blocks represent 8x8 pixels in horizontal and vertical strips, pixels are in rows and columns). Therefore, Anesko meets the claimed features.

Conclusion

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung T. Vo whose telephone number is (703) 308-5874. The examiner can normally be reached on 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris. Kelley can be reached on (703) 305-4856. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TUNG T VO
PATENT EXAMINER

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Art Unit 2613

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